REMARKS

Claim 1 have been amended. No claims have been cancelled. No claims have been added. Hence claims 1-8 are pending.

The informal drawings are objected to. Formal drawings have been submitted concurrently with the instant amendment. Consequently, the objection to the drawings should be withdrawn.

The specification has been amended. While preparing the formal drawings it was necessary to split Fig. 4 into Figs. 4A and 4B. Similarly, Fig. 14 was also split into Figs. 14A and 14B. Accordingly, the Brief Description of the Drawings have been amended to additionally describe Figs. 4A, 4B, 14A, and 14B.

Claims 1-3 and 8 stand rejected under 35 U.S.C. 102(e) as being anticipated by Gowda (U.S. Patent No. 6,115,066). Claim 4 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda in view of Ando (U.S. Patent No. 4,839,729). Claims 5-7 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gowda in view of Adiletta (U.S. Patent No. 6,295,546). These rejections are respectfully traversed.

The present invention is directed to an image sensor system having a plurality of analog-to-digital ("A/D") converters each associated with a plurality of logical units. Each logical unit is comprised of a group of pixels. In one exemplary embodiment, the logical units are the columns of the pixel array. Specification, p. 28. However, logical units in alternate embodiment may instead be rows, or any other structures comprising plural pixels. Specification, p. 31. Each A/D converter additionally includes a plurality of storage locations. Each storage location is used to store the digital value converted from an analog signal of a pixel in a logical unit associated with that A/D converter.

The association between a single A/D converter and multiple logical units is often made in order to reduce the amount of required circuitry. For example, A/D converters are often shared between adjacent columns. In many instances, it is desirable to

read the converted digital value in the same order as its placement. For example, it may be desirable to read digital values of each adjacent column of a row. However, the A/D conversion process requires a finite amount of time and triggering shared A/D converters in the same order as the desired read order can result is slow performance due to the requirement to wait the finite amount of time between each conversion.

In the present invention, each A/D converter is associated with a plurality of logical units and each A/D converter is also associated with a plurality of storage locations each capable of storing a single converted digital value. Each storage location is capable of storing a single converted digital value. For example, if the A/D converter produces an 8-bit digital value, the A/D converter would be associated with at least two storage locations and each location would be capable of storing 8-bits of data. See, e.g., specification, p. 29. For example, in the portion of claim 1 which is quoted below, an analog signal from a pixel is converted into a "converted digital value" which is stored in one of a plurality of associated storage elements.

The storage locations also permit the A/D converted values to be read in a desired read order which may be different from a conversion order. For example, if each A/D converter were associated with two adjacent columns, each A/D converter can be controlled to first convert and store a pixel signal from an odd column and then to convert and store a pixel signal from an even column. The converted value can then be read in column order by reading the storage locations in the desired order.

Accordingly, the independent claims 1 and 5 include limitations directed to an A/D converter having plural storage units. More specifically, claim 1 recites:

> a plurality of analog-to-digital converters ... each associated with N logical units ..., each of said N logical units having including a plurality of pixels, wherein each analog-to-digital converter includes an ADC portion which receives an analog signal from one of said pixel sensors of an associated logical unit when a selector element associated with said one pixel is enabled, and converts said analog signal to a converted digital value indicating the output

signal, and said ADC portion stores said converted digital value into one of a plurality of associated storage elements

Claim 5 similarly recites:

receiving, in a plurality of A/D converter units, a respective plurality of signals from a respective plurality of first logical units, and A/D converting said respective plurality of signals into a respective plurality of converted digital values and storing said respective plurality of converted digital values information in a respective plurality of first storage units;

receiving, in said plurality of A/D converter units, a respective of signals from a respective plurality of second logical units, adjacent to said first logical units, and A/D converting said respective plurality of signals into a respective plurality of converted digital values and storing said respective plurality of converted digital values in a respective plurality of second storage units

reading out said information from said A/D conversion unit in a different order than an order in which the information was converted.

Gowda is directed to a image sensor architecture. As shown in Fig. 3, Gowda discloses a image sensor architecture in which the pixels 30 of the image sensor are organized into columns $C_1 \ldots C_n$, wherein each column of pixels is associated with a respective column line $15_1 \ldots 15_n$. Associated with each column line $15_1 \ldots 15_n$ is an A/D converter $40_1 \ldots 40_n$. Each A/D converter $40_1 \ldots 40_n$ is coupled to a register $42_1 \ldots 42_n$. Significantly, each one of the A/D converter $40_1 \ldots 40_n$ is coupled only a respective one of the plurality of register $42_1 \ldots 42_n$. As such, the image sensor architecture of Gowda does not teach or suggest an apparatus wherein "a plurality of analog-to-digital converters ... each associated with N logical units ..., each of said N logical units having including a plurality of pixels, wherein each analog-to-digital converter includes an ADC portion which receives an analog signal from one of said pixel sensors of an associated logical unit when a selector element associated with said one pixel is enabled, and converts said analog signal to a converted digital value indicating the output signal, and said

ADC portion stores said converted digital value into one of a plurality of associated storage elements" as required by independent claim 1. Similarly, Gowda does not teach or suggest the steps of "receiving, in a plurality of A/D converter units, a respective plurality of signals from a respective plurality of first logical units, and A/D converting said respective plurality of signals into a respective plurality of converted digital values and storing said respective plurality of converted digital values information in a respective plurality of first storage units" and "receiving, in said plurality of A/D converter units, a respective of signals from a respective plurality of second logical units, adjacent to said first logical units, and A/D converting said respective plurality of signals into a respective plurality of converted digital values and storing said respective plurality of converted digital values in a respective plurality of second storage units."

Ando is directed to a solid state image sensor including separate "memories" for storing bright and dark signals from a light receiving section. A differential amplifier 18 (Figs. 2-3) is used to remove fixed pattern noise. The output of the differential amplifier 18 corresponds to the analog signal which is A/D converted to produce a converted digital value in claims 1 and 5. As such Ando also fails to teach or disclose the above cited limitations of independent claims 1 and 5.

Adiletta is directed to a method for performing data scattering and retrieval such that certain calculations which normally require the use of a double ported memory can be performed using a single ported memory. Adieletta further discloses a method for performing discrete cosine transformation without requiring the use of a transpose matrix buffer. The Office Action cites a portion of Adieletta directed to big/little endian data format conversion for a teaching of reading information from an analog-to-digital converter in a different order in which the information was converted. However, Adieletta, like Gowda and Ando, fails to teach or suggest the above recited limitations of the independent claims.

Claims 1 and 5 are therefore believed to be allowable over the prior art of record. Claims 2-4 and 8 (which depend from claim 1) and claims 6-7 (which depend from claim 5) are also believed to be allowable for these reasons and because the combination recited in the claims are not taught or suggested by the prior art of record.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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